

# M61520FP

## 6ch Electronic Volume with Tone Control

REJ03F0057-0100Z

Rev.1.0

Sep.19.2003

### Features

Function names	Features
Volume	Six independent high-performance independent volumes on-chip (0 to 87 dB in 1 dB steps, $-\infty$ )
Input selector	L/R ch: 6 inputs with muting and attenuation
REC output	Two-channel record output (one channel includes a mute switch)
Gain control	Input gain control for FL, FR, C, SL, SR, and SW channels (0/3.6 dB) Record-input gain control (+1/+3/+4.6/+6.6 dB) Output gain control for SL, SR and C channels (0/+6 dB) Output gain control for the SW channel (+6/+10 dB) Output gain control for FL and FR channels (0/+2/+6.5/+10.5 dB) *1 Microphone-mix gain control (0/-2/+6.5/+10.5 dB) *1
Bass boost	On-chip bass-boost circuits for the FL and FR channels
Balanced output	Internal balanced outputs for the ADC

Note: 1 The microphone mix gain is coupled with output gain control for the FL and FR channels.

### Application

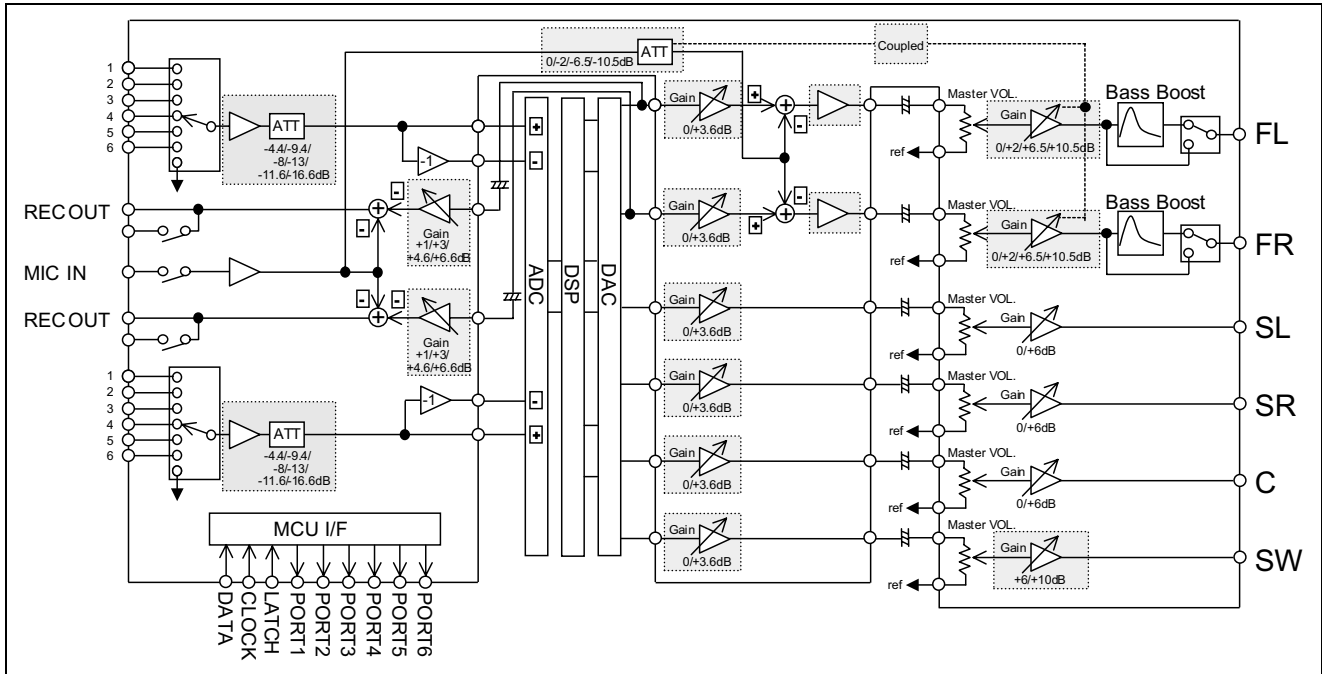
Mini-component systems, TVs, etc.

### Recommended Operating Conditions

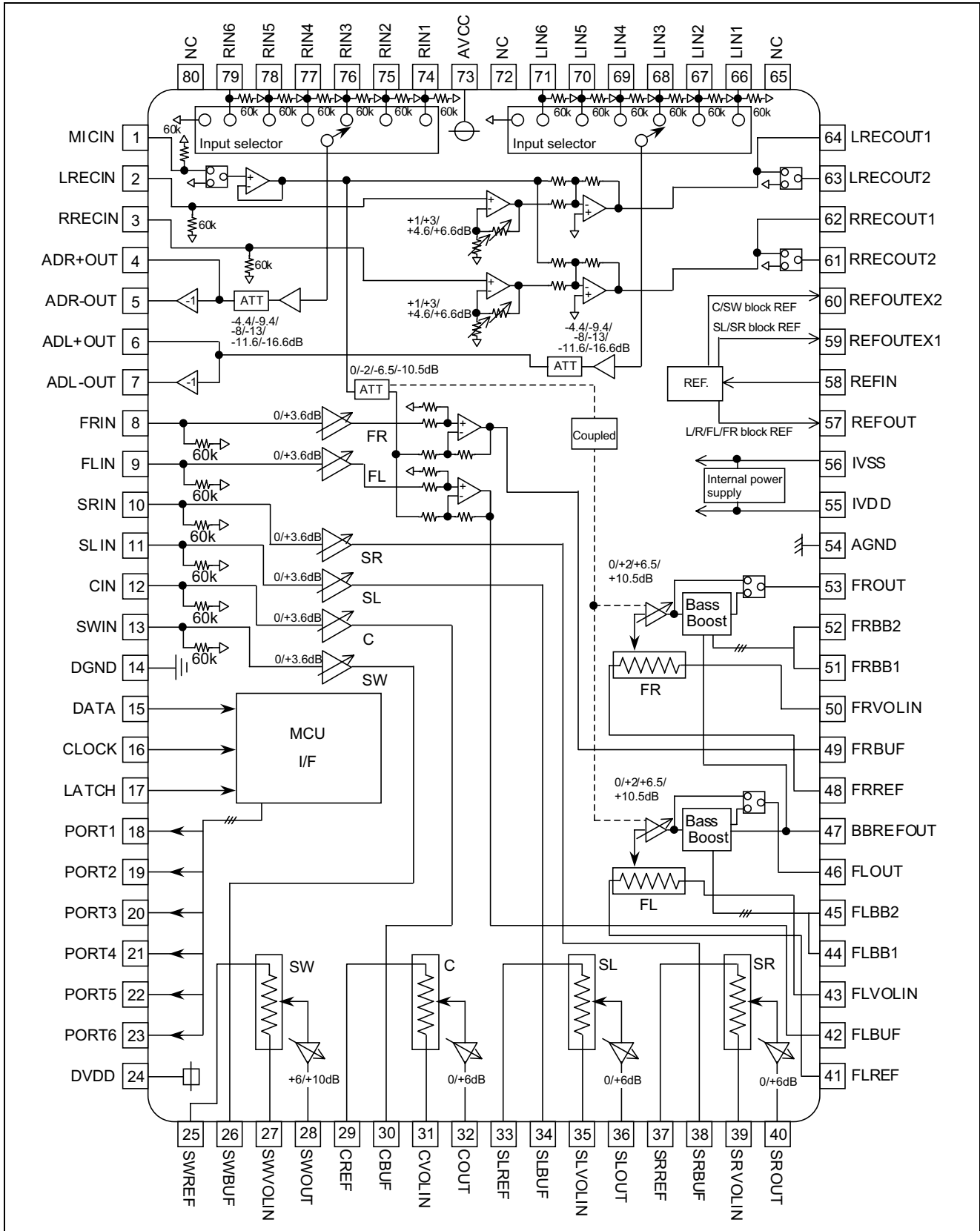
Analog power-supply voltage range: 8.0 V to 10.0 V

Digital power-supply voltage range: 3.0 V to 5.5 V

System Block Diagram

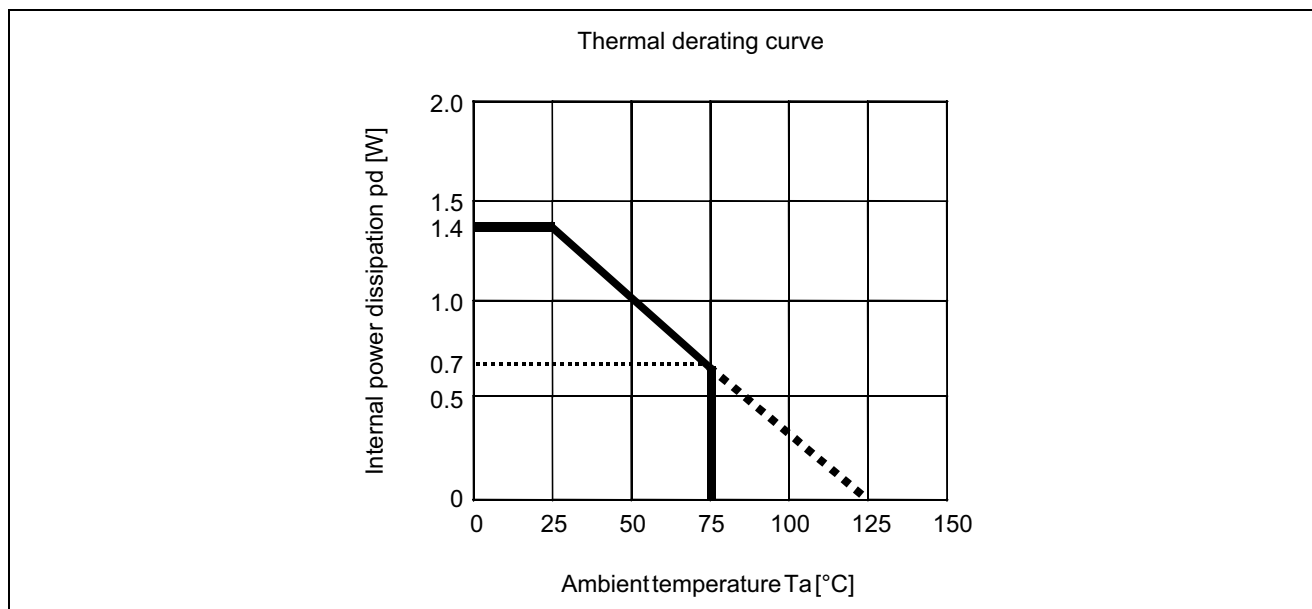


Block Diagram with Pin Connections



## Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Conditions
Max. power-supply voltage	AVCC	10.5	V	
	DVDD	6.5	V	
Internal power dissipation	Pd	1.4	W	
Ambient operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	



## Recommended Operating Condition

Item	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Power-supply voltage	AVCC	8.0	9.0	10.0	V	
	DVDD	3.0	5.0	5.5	V	
Input voltage (L level)	VIL	0.0	—	0.8	V	Pins 15, 16, and 17
Input voltage (H level)	VIH	2.0	—	VDD	V	Pins 15, 16, and 17

## Electrical characteristics

Unless otherwise noted, Ta = 25°C, AVCC = 9.0 V, DVDD = 5.0 V, f = 1 kHz, and bass boosting is switched off.

### (1) Power-supply characteristics

Item	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Analog power-supply circuit current	AICC	—	20	40	mA	Current on pin 73 when AVCC = 5 V, with no signal
Digital power-supply circuit current	Didd	—	0.8	1.5	mA	Current on pin 24 when DVDD = 5 V, with no signal

## (2) Input/output characteristics

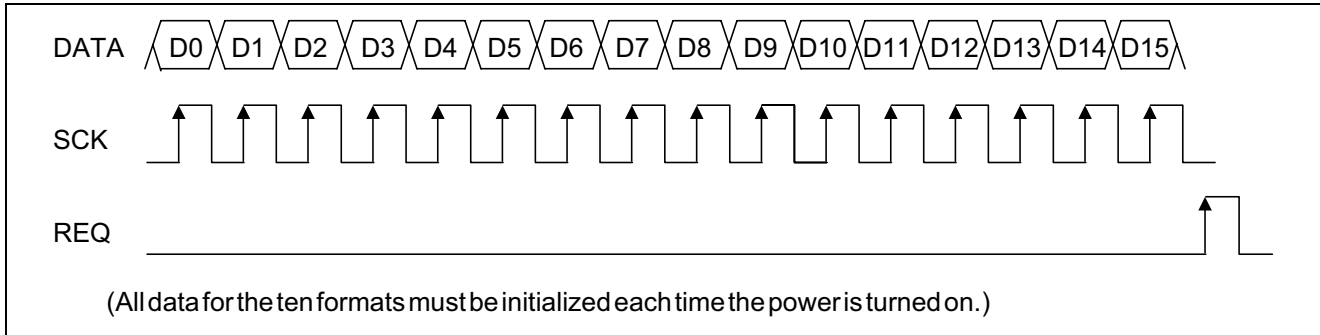
Item	Symbol	Limits			Unit	Condition	
		Min.	Typ.	Max.			
Input impedance	Rin	30	60	90	K $\Omega$	66pin, 74pin	
Input-selector max. input voltage	Vin	1.8	2.2	—	Vrms	66pin, 74pin	
FL, FR OUT max. output voltage	Vom	1.8	2.2	—	Vrms	Input on pins 8 and 9, output on pins 46 and 53, RL = 10 k $\Omega$ , THD = 1%, bass boost = on, fin = 80 Hz	
REC OUT max. output voltage	Vomrec	1.8	2.2	—	Vrms	Input on pins 2 and 3, output on pins 62 and 64, RL = 10 k $\Omega$ , THD = 1%, fin = 1 kHz	
C, SL, SR, SW max. output voltage	Vomvol	1.8	2.2	—	Vrms	Input on pins 10 and 11, output on pins 36 and 40. RL = 10 k $\Omega$ , THD = 1%, fin = 1 kHz, gain = 6 dB	
Bypass gain 1	Gv1	—	-8.0	—	dB	Gain from pins 4 to 74 and pins 6 to 66.	
Bypass gain 2	Gv2	—	0	—	dB	Gain from pins 8 to 53 and pins 9 to 46.	
Max. attenuation	ATT	-87	-92	—	dB	Vo = 1 Vrms, on pins 40 and 36, JIS-A filter	
ADOUT output noise voltage	Vadno	—	4.0	12.0	$\mu$ Vrms	JIS-A filter, when no signal is present, RG = 10 k $\Omega$ , on pins 4 and 6, "normal function" settings	
RECOU output noise voltage	Vrecno	—	7.0	15.0	$\mu$ Vrms	JIS-A filter, when no signal is present, RG = 10 k $\Omega$ , on pins 62 and 64, "normal function" settings	
FL, FROUT output noise voltage	Vono1	—	7.0	15.0	$\mu$ Vrms	JIS-A filter, when no signal is present, Rg = 10 k $\Omega$ , volume setting: 0 dB, "normal function" settings	46, 53pin
C, SL, SRVOLOUT output noise voltage	Vvolno1	—	6.0	12.0	$\mu$ Vrms	JIS-A filter, when no signal is present, Rg = 10 k $\Omega$ , volume setting: 0 dB, "normal function" settings	40, 36pin
SW VOLOUT output noise voltage	Vvolwno1	—	12.0	24.0	$\mu$ Vrms	JIS-A filter, when no signal is present, Rg = 10 k $\Omega$ , volume setting: 0 dB, "normal function" settings	28pin
FL, FROUT output noise voltage	Vono2	—	5.0	10.0	$\mu$ Vrms	JIS-A filter, when no signal is present, Rg = 10 k $\Omega$ , volume setting: $-\infty$ dB, "normal function" setting	46, 53pin
C, SL, SRVOLOUT output noise voltage	Vvolno2	—	4.0	8.0	$\mu$ Vrms	JIS-A filter, when no signal is present, Rg = 10 k $\Omega$ , volume setting: $-\infty$ dB, "normal function" setting	40, 36pin
SW VOLOUT output noise voltage	Vvolwno2	—	8.0	16.0	$\mu$ Vrms	JIS-A filter, when no signal is present, Rg = 10 k $\Omega$ , volume setting: $-\infty$ dB, "normal function" setting	28pin
Distortion on FL, FROUT	THD	—	0.01	0.05	%	On pins 46 and 53, BW = 400 to 30 kHz, Vo = 300 mVrms, RL = 30 k $\Omega$	
Distortion on REC OUT	THDrec	—	0.01	0.05	%	On pins 62 and 64, BW = 400 to 30 kHz, Vo = 300 mVrms, RL = 51 k $\Omega$	
Distortion on C, SL, SR, SWVOLOUT	THDvol	—	0.01	0.05	%	On pins 40 and 36, BW = 400 to 30 kHz, Vo = 300 mVrms, RL = 30 k $\Omega$	
Crosstalk between channels	CT	—	-70	-55	dB	Vo = 0.5 Vrms, RL = 10 k $\Omega$ , JIS-A, Rg = 10 k $\Omega$ , between pins 46 and 53	
	CTrec	—	-70	-55	dB	Vo = 0.5 Vrms, RL = 30 k $\Omega$ , JIS-A, Rg = 10 k $\Omega$ , between pins 62 and 64	

**Normal function settings:**

- Input attenuator: -8 dB
- REC input gain amp: +1 dB
- FL, FR, C, SL, SR, SW input gain amp: 0 dB
- SL, SR, C output gain amp: 0 dB
- SW output gain amp: +6 dB

**Specification of Control Data**

Data is fetched on rising edges of SCK; after 16 bits have been fetched, they are internally latched on the rising edge of REQ.

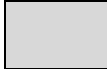


	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
A	0	0	0	0	(1) Input selector			(2) Input ATT			(3) REC inGain	(4) FL/FR inGain	(5) SL/SR/C/SW inGain			Chip address 1 1	
B	0	0	0	1	(6) MIC MIX/FL/FR Gain		(7) SL/SR/C Gain	(8) SW Gain	(9) PORT1	(10) PORT2	(11) PORT3	(12) PORT4	(13) PORT5	(14) PORT6			
C	1	0	0	0	(15) ALL MUTE	(16) MIC MUTE	(17) REC2 MUTE	(19) Lch volume									
D	1	0	0	1	0	0	(18) Bass Boost	(19) Rch volume									
E	1	0	1	0	0	0	0	(19) Cch volume									
F	1	0	1	1	0	0	0	(19) SLch volume									
G	1	1	0	0	0	0	0	(19) SRch volume									
H	1	1	0	1	0	0	0	(19) SWch volume									

**Initial internal state of the IC (state just after power is turned on):**

- (1) Input selector : MUTE (9) OUTPUTPORT1 : PORT1OFF (18) Bass boost: No boost
- (2) Input ATT : -8dB (10) OUTPUTPORT2 : PORT2OFF (19) LchVOL : -∞dB
- (3) Record-input gain amp : +1dB (11) OUTPUTPORT3 : PORT3OFF (20) RchVOL : -∞dB
- (4) FL/FRch input gain amp : 0dB (12) OUTPUTPORT4 : PORT4OFF (21) CchVOL : -∞dB
- (5) SL/SR/C/SWch input gain amp : 0dB (13) OUTPUTPORT5 : PORT5OFF (22) SLchVOL : -∞dB
- (6) MIC mixing gain, (14) OUTPUTPORT6 : PORT6OFF (23) SRchVOL : -∞dB  
FL/FR output gain amp : 0dB (15) Mute all : No muting (24) SWchVOL : -∞dB
- (7) SL/SR/Cch output gain amp : 0dB (16) MIC MUTE : MUTE
- (8) SWch output gain amp : +6dB (17) REC2 MUTE : THRU

Note: Do not input values other than those specified above. Operation is not guaranteed with other values.

◆  Setting just after power is turned on

(1) Input selector setting

INPUT SEL.	D4A	D5A	D6A
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
MUTE	1	1	1

(7) SL/SR/C ch output gain amp setting

SL/SR/C GAIN AMP	D6B
0	0
+6dB	1

(15) Mute-all setting

ALL MUTE
No MUTE
ALL MUTE

(2) Input ATT setting

INPUT ATT	D7A	D8A	D9A
-8dB	0	0	0
-13 dB	0	0	1
-4.4 dB	0	1	0
-9.4 dB	0	1	1
-11.6 dB	1	0	0
-16.6 dB	1	0	1

(8) SW ch output gain amp setting

SW GAIN AMP	D7B
+6dB	0
+10dB	1

(16) Microphone mute setting

MIC MUTE
THRU
MUTE

(3) REC input gain amp setting

REC IN GAIN	D10A	D11A
+1 dB	0	0
+3 dB	0	1
+4.6 dB	1	0
+6.6 dB	1	1

(9) Output port 1 setting

PORT1	D8B
PORT1 OFF	0
PORT1 ON	1

(17) RECOUT2 mute setting

REC2 MUTE
THRU
MUTE

(10) Output port 2 setting

PORT2	D9B
PORT2 OFF	0
PORT2 ON	1

(18) Bass-boost setting

BASS BOOST
No Boost
Boost ON

(4) FL/FR ch input gain amp setting

FL/FR IN GAIN	D12A
0 dB	0
+3.6 dB	1

(11) Output port 3 setting

PORT3	D10B
PORT3 OFF	0
PORT3 ON	1

(12) Output port 4 setting

PORT4	D11B
PORT4 OFF	0
PORT4 ON	1

(5) SL/SR/C/SW ch input gain amp setting

SL/SR/C/SW IN GAIN	D13A
0 dB	0
+3.6 dB	1

(13) Output port 5 setting

PORT5	D12B
PORT5 OFF	0
PORT5 ON	1

(14) Output port 6 setting


PORT6	D13B
PORT6 OFF	0
PORT6 ON	1

(6) MIC mixing gain, FL/FR ch output gain setting

MIC MIX GAIN	FL/FR GAIN AMP	D4B	D5B
0 dB	0 dB	0	0
-2 dB	+2 dB	0	1
-6.5 dB	+6.5 dB	1	0
-10.5 dB	+10.5 dB	1	1

(19) Volume setting

(FLch, FRch, SLch, SRch, SWch)

◆  Setting just after power is turned on

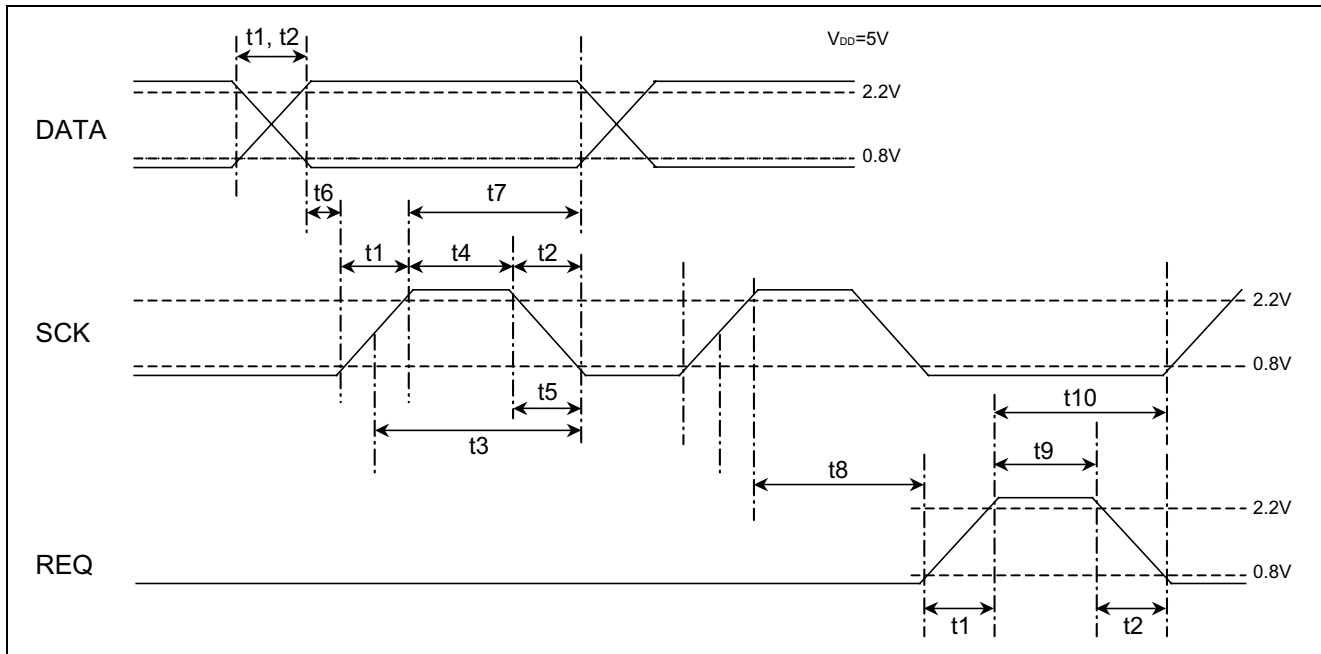
ATT	D7C-H	D8C-H	D9C-H	D10C-H	D11C-H	D12C-H	D13C-H
±0dB	0	0	0	0	0	0	0
-1.0dB	1	0	0	0	0	0	0
-2.0dB	0	1	0	0	0	0	0
-3.0dB	1	1	0	0	0	0	0
-4.0dB	0	0	1	0	0	0	0
-5.0dB	1	0	1	0	0	0	0
-6.0dB	0	1	1	0	0	0	0
-7.0dB	1	1	1	0	0	0	0
-8.0dB	0	0	0	1	0	0	0
-9.0dB	1	0	0	1	0	0	0
-10.0dB	0	1	0	1	0	0	0
-11.0dB	1	1	0	1	0	0	0
-12.0dB	0	0	1	1	0	0	0
-13.0dB	1	0	1	1	0	0	0
-14.0dB	0	1	1	1	0	0	0
-15.0dB	1	1	1	1	0	0	0
-16.0dB	0	0	0	0	1	0	0
-17.0dB	1	0	0	0	1	0	0
-18.0dB	0	1	0	0	1	0	0
-19.0dB	1	1	0	0	1	0	0
-20.0dB	0	0	1	0	1	0	0
-21.0dB	1	0	1	0	1	0	0
-22.0dB	0	1	1	0	1	0	0
-23.0dB	1	1	1	0	1	0	0
-24.0dB	0	0	0	1	1	0	0
-25.0dB	1	0	0	1	1	0	0
-26.0dB	0	1	0	1	1	0	0
-27.0dB	1	1	0	1	1	0	0
-28.0dB	0	0	1	1	1	0	0
-29.0dB	1	0	1	1	1	0	0
-30.0dB	0	1	1	1	1	0	0
-31.0dB	1	1	1	1	1	0	0
-32.0dB	0	0	0	0	0	1	0
-33.0dB	1	0	0	0	0	1	0
-34.0dB	0	1	0	0	0	1	0
-35.0dB	1	1	0	0	0	1	0
-36.0dB	0	0	1	0	0	1	0
-37.0dB	1	0	1	0	0	1	0
-38.0dB	0	1	1	0	0	1	0
-39.0dB	1	1	1	0	0	1	0
-40.0dB	0	0	0	1	0	1	0
-41.0dB	1	0	0	1	0	1	0
-42.0dB	0	1	0	1	0	1	0
-43.0dB	1	1	0	1	0	1	0
-44.0dB	0	0	1	1	0	1	0

ATT	D7C-H	D8C-H	D9C-H	D10C-H	D11C-H	D12C-H	D13C-H
-45.0dB	1	0	1	1	0	1	0
-46.0dB	0	1	1	1	0	1	0
-47.0dB	1	1	1	1	0	1	0
-48.0dB	0	0	0	0	1	1	0
-49.0dB	1	0	0	0	1	1	0
-50.0dB	0	1	0	0	1	1	0
-51.0dB	1	1	0	0	1	1	0
-52.0dB	0	0	1	0	1	1	0
-53.0dB	1	0	1	0	1	1	0
-54.0dB	0	1	1	0	1	1	0
-55.0dB	1	1	1	0	1	1	0
-56.0dB	0	0	0	1	1	1	0
-57.0dB	1	0	0	1	1	1	0
-58.0dB	0	1	0	1	1	1	0
-59.0dB	1	1	0	1	1	1	0
-60.0dB	0	0	1	1	1	1	0
-61.0dB	1	0	1	1	1	1	0
-62.0dB	0	1	1	1	1	1	0
-63.0dB	1	1	1	1	1	1	0
-64.0dB	0	0	0	0	0	0	1
-65.0dB	1	0	0	0	0	0	1
-66.0dB	0	1	0	0	0	0	1
-67.0dB	1	1	0	0	0	0	1
-68.0dB	0	0	1	0	0	0	1
-69.0dB	1	0	1	0	0	0	1
-70.0dB	0	1	1	0	0	0	1
-71.0dB	1	1	1	0	0	0	1
-72.0dB	0	0	0	1	0	0	1
-73.0dB	1	0	0	1	0	0	1
-74.0dB	0	1	0	1	0	0	1
-75.0dB	1	1	0	1	0	0	1
-76.0dB	0	0	1	1	0	0	1
-77.0dB	1	0	1	1	0	0	1
-78.0dB	0	1	1	1	0	0	1
-79.0dB	1	1	1	1	0	0	1
-80.0dB	0	0	0	0	1	0	1
-81.0dB	1	0	0	0	1	0	1
-82.0dB	0	1	0	0	1	0	1
-83.0dB	1	1	0	0	1	0	1
-84.0dB	0	0	1	0	1	0	1
-85.0dB	1	0	1	0	1	0	1
-86.0dB	0	1	1	0	1	0	1
-87.0dB	1	1	1	0	1	0	1
-∞dB	1	1	1	1	1	1	1

Note: Do not input values other than those specified above. Operation is not guaranteed with other values.



## Control-Data Timing

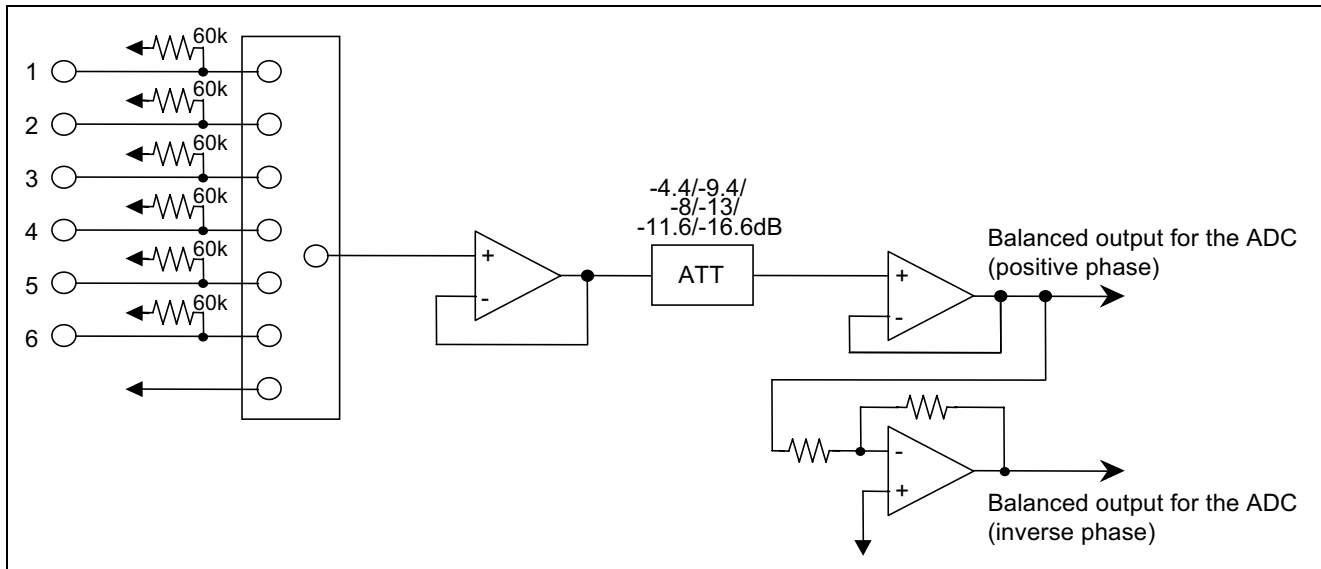


Name	Symbol	Min.	Typ.	Max.	Unit
Time for signal to rise	t1	—	—	0.3	$\mu\text{s}$
Time for signal to fall	t2	—	—	0.3	$\mu\text{s}$
SCK clock width	t3	1	—	—	$\mu\text{s}$
SCK high pulse width	t4	0.4	—	—	$\mu\text{s}$
SCK low pulse width	t5	0.4	—	—	$\mu\text{s}$
DATA setup time	t6	0.4	—	—	$\mu\text{s}$
DATA hold time	t7	0.4	—	—	$\mu\text{s}$
REQ rise hold time	t8	0.8	—	—	$\mu\text{s}$
REQ high pulse width	t9	0.4	—	—	$\mu\text{s}$
SCK setup time	t10	0.4	—	—	$\mu\text{s}$

## Functional description

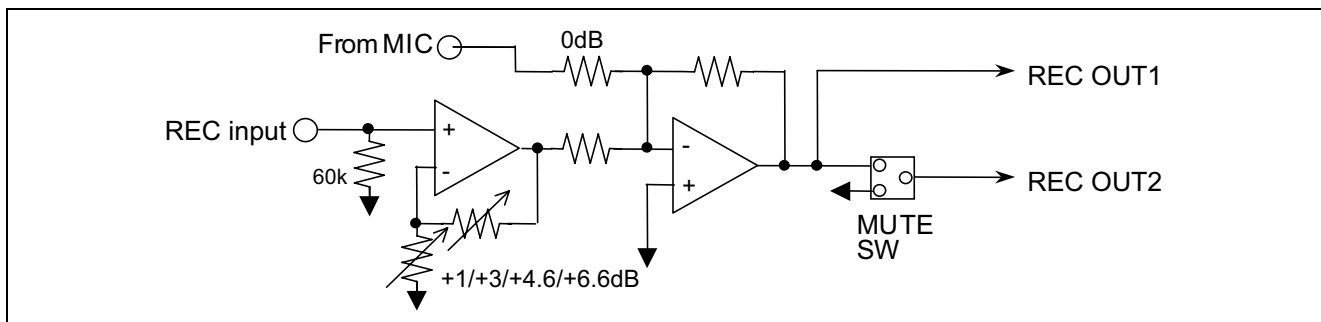
### (1) Input selector, input attenuator

The IC incorporates a selector for either of two six-input channels and a mute switch. An input level for the selected input is chosen from among -4.4, -8, -9.4, -11.6, -13, and -16.6 dB.



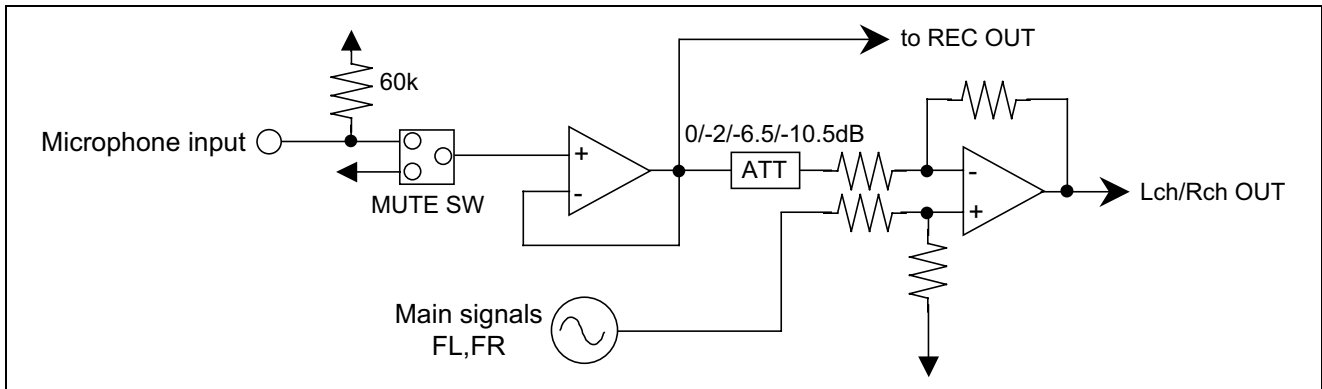
### (2) REC block

The REC signal is mixed with the MIC signal and then output. The gain of the signal for mixing with the MIC signal is selected from among +1 dB, +3, +4.6, +6.6 dB. The REC OUT2 side includes a mute switch.



(3) Microphone mixing

In the microphone-input circuit, the input signal is passed through an op-amp buffer to prevent crosstalk between FL and FR and then mixed with FL and FR. The level of the mixed signal changes in accordance with the variable gain of the output gain amplifier (see the table below). A mute switch is incorporated to improve noise characteristics when microphone mixing is not in use.



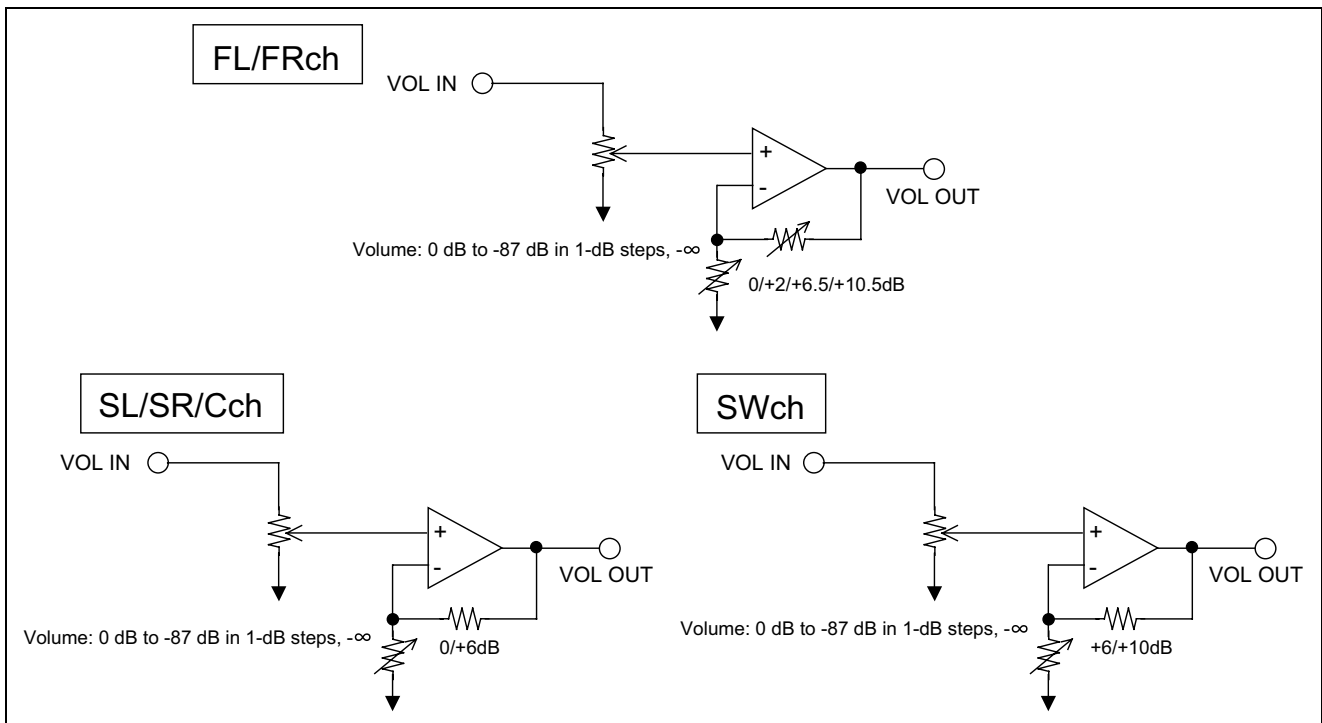
The relation between the output gain and mixing gain

FL/FR output gain	Mixing gain
0	0
+2dB	-2dB
+6.5dB	-6.5dB
+10.5dB	-10.5dB

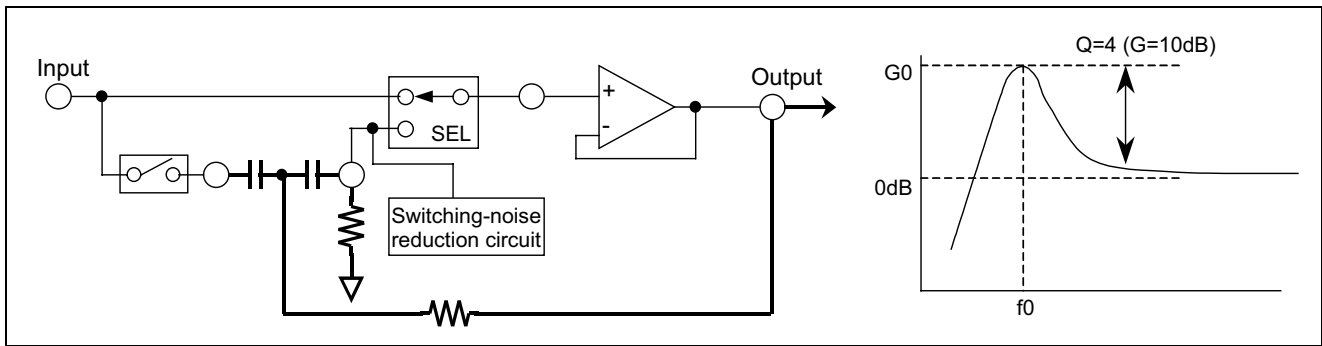
(4) Master volume (FL ch, FR ch, C ch, SL ch, SR ch, SW ch)

This IC incorporates six independently controlled electronic volumes, each of which has low-distortion and low-noise characteristics.

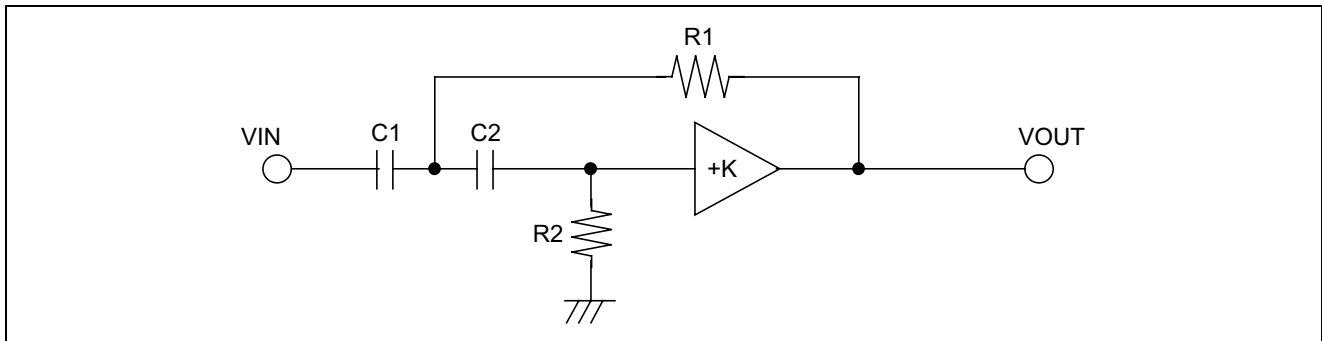
Volume: attenuation of 0 dB to -87 dB, settable in 1-dB steps.



(5) Equivalent Circuit for the Bass-Boost Circuit



Positive-feedback second-order high-pass filter circuit for the bass-boost module



Amplitude characteristics of the second-order high-pass filter

Q	G0
1	0 to 1dB
2	6dB
4	10dB
5	13dB
10	20dB

The transfer function is described by the following expressions:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Ks^2}{s^2 + s \left[ \frac{1}{R_2C_1} + \frac{1}{R_2C_2} + (1-K) \frac{1}{R_1C_1} \right] + \frac{1}{R_1R_2C_1C_2}}$$

$$\omega_0^2 = \frac{1}{R_1R_2C_1C_2}$$

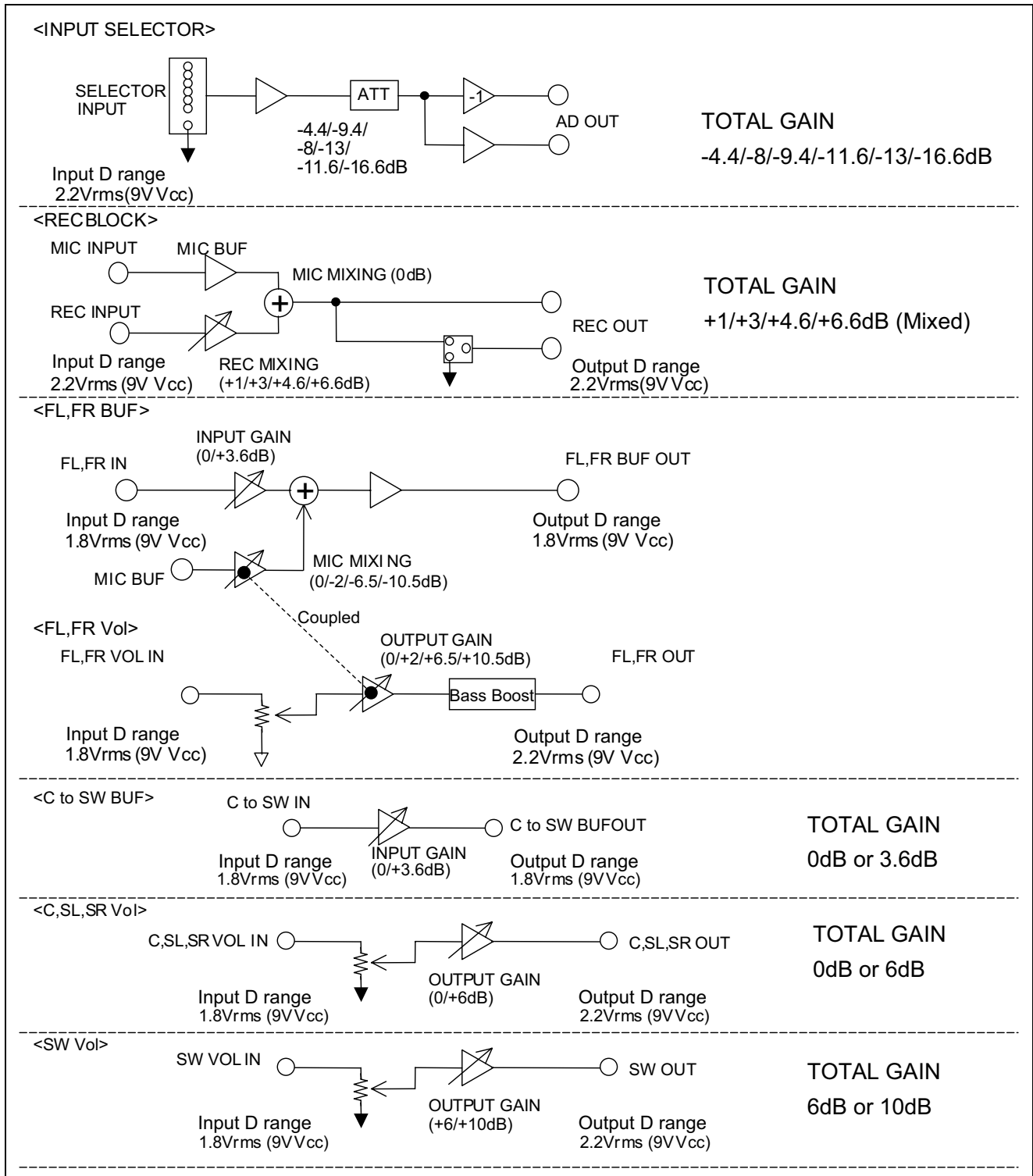
$$Q = \frac{1}{\sqrt{\frac{R_1C_1}{R_2C_2} + \sqrt{\frac{R_1C_2}{R_2C_1} + (1-K) \sqrt{\frac{R_2C_2}{R_1C_1}}}}$$

The bass-boost module includes the above positive-feedback second-order high-pass filter.

In the above figure, when  $R_1 = 1.2 \text{ k}\Omega$ ,  $R_2 = 470 \text{ k}\Omega$ , and  $C_1 = C_2 = 0.1 \text{ }\mu\text{F}$  ( $K = +1$ ),

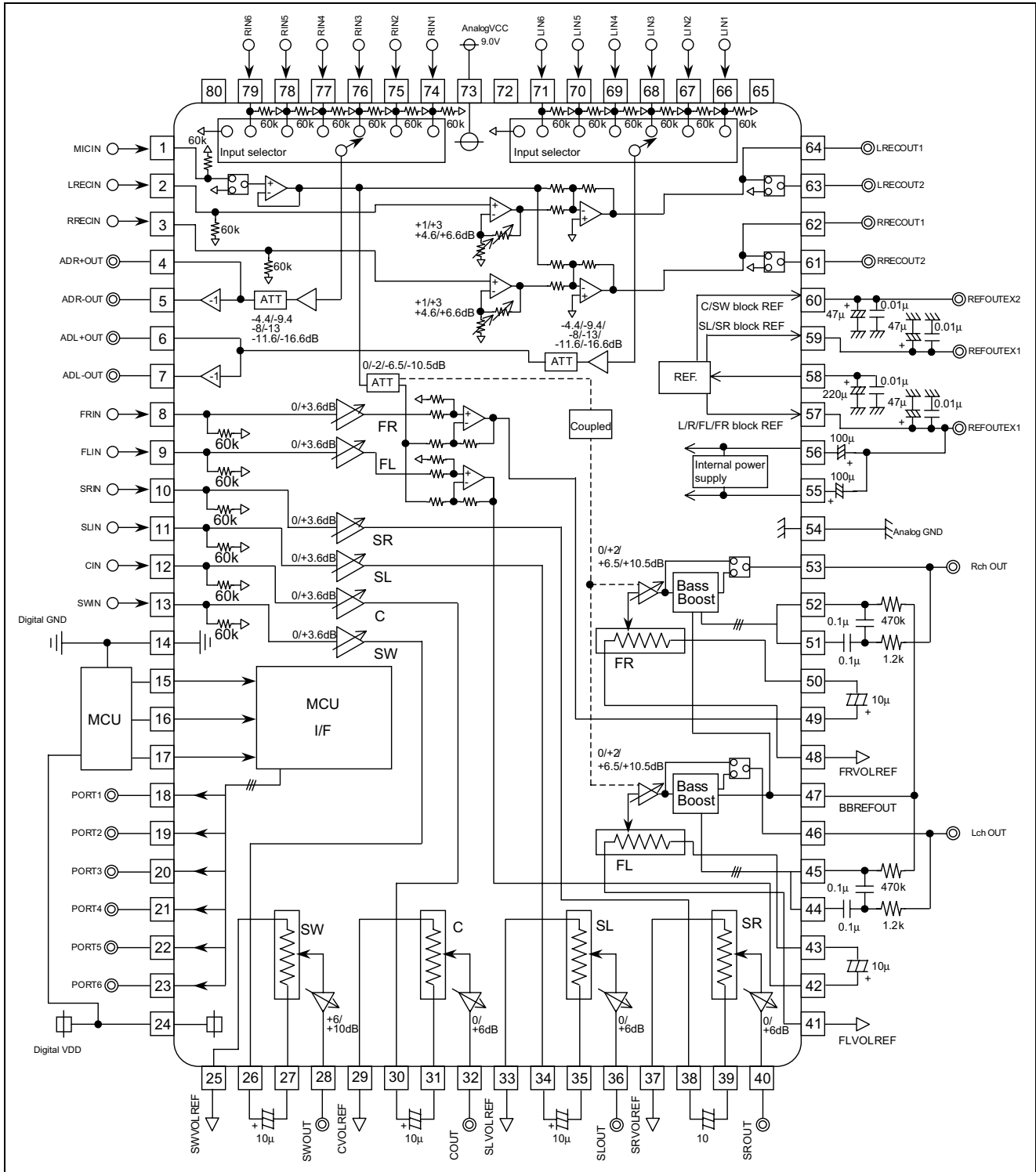
$f_0 = 70 \text{ Hz}$  ( $f_0 = \omega_0/2\pi$ ),  $Q = 10$ .

Gain Level Diagram



Caution: Do not input a signal which exceeds the power-supply voltage level.

Application Example



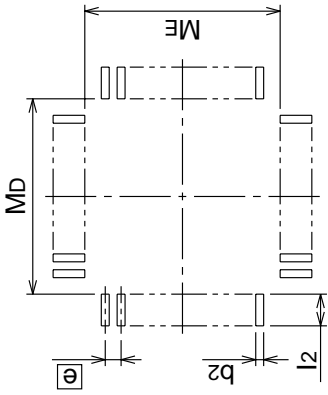
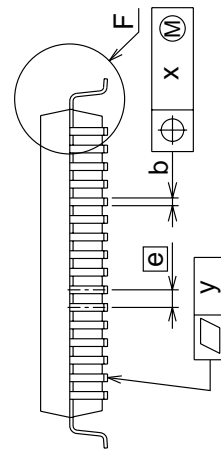
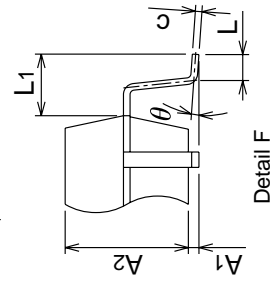
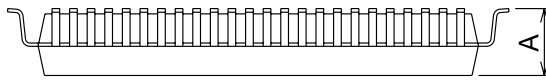
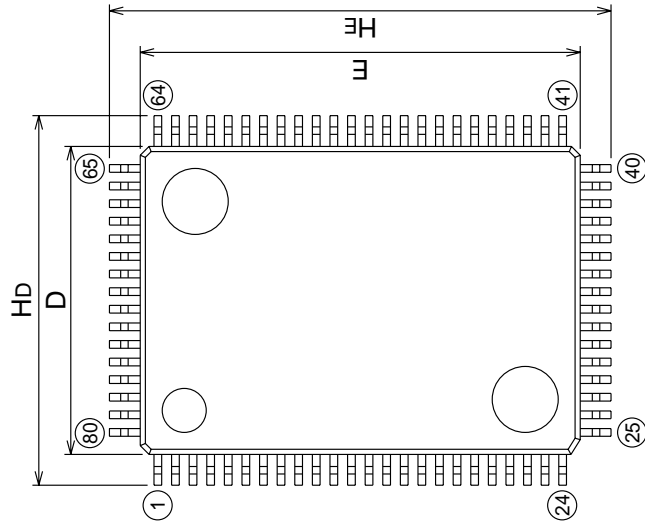
Package Dimensions

**80P6N-A**

(MMP)

**Plastic 80pin 14X20mm body QFP**

EIAJ Package Code QFP80-P-1420-0.80	JEDEC Code —	Weight(g) 1.58	Lead Material Alloy 42
--	-----------------	-------------------	---------------------------



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	—	1.4	—
x	—	—	0.2
y	—	—	0.1
$\theta$	0°	—	10°
b2	—	0.5	—
l2	1.3	—	—
MD	—	14.6	—
ME	—	20.6	—

## RENESAS Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

---

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
  2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
  3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
  4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
  5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
  6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
  7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
  8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
- 



### RENESAS SALES OFFICES

<http://www.renesas.com>

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited.**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom  
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

**Renesas Technology Europe GmbH**  
Dornacher Str. 3, D-85622 Feldkirchen, Germany  
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

**Renesas Technology Hong Kong Ltd.**  
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2375-6836

**Renesas Technology Taiwan Co., Ltd.**  
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**  
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**  
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001